## REMARKS

Claims 1-28 are presented for consideration in the present application, which is now believed to be in condition for examination. Early notice to that effect is earnestly solicited.

Respectfully submitted,

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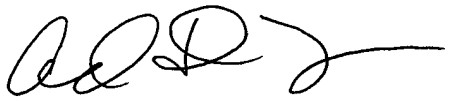

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be readily achieved by use of the VERILOG® description along with circuitry to provide interfacing to the base station and the device under test (DUT).

Please replace the paragraph beginning at page 20, line 17 with the following:

Data transfer continues in this manner until the FPGA 220 is fully programmed by virtue of having received the correct amount of data required by the particular FPGA 220 used in base station 218. Thus, each time the host software is initialized, a data transfer to the FPGA 220 occurs to program the FPGA 220 to function in its capacity of a virtual microcontroller (in this embodiment). Once programming ceases, the FPGA 220 operates as a virtual microcontroller (or whatever device is programmed into the FPGA 220 in general). At this point, the interface 214 ceases to function as a unidirectional programming interface and begins to function as a bidirectional communication interface using the programmed operation of the FPGA 220 communicating through its programmed IEEE 1284 EPP parallel communication interface.

VERSION OF AMENDMENTS WITH CHANGES SHOWN:

IN THE SPECIFICATION

Please replace the paragraph beginning at page 12, line 2 with the following:

Referring now to FIGURE 1, a system 200 is shown that includes a host computer 210 (e.g., a personal computer based on a [Pentium™] PENTIUM® class microprocessor) that is interconnected (e.g., using a standard PC interface 214 such as a parallel printer port connection, a universal serial port (USB) connection, etc.) with a base station 218. The host computer 210 generally operates to run an ICE computer program to control the emulation process and further operates in the capacity of a logic analyzer to permit a user to view information provided from the base station 218 for use in analyzing and debugging a system under test or development.

Please replace the paragraph beginning at page 13, line 5 with the following:

In one embodiment, system 200 is adapted to test the CY8C25xxx/26xxx series of microcontrollers made by Cypress [Micro Systems,] MicroSystems, Inc., 22027 17th Avenue SE, Suite 201, Bothell, WA [98021Bothell, WA] 98021. In this embodiment FPGA 220 emulates the core processor functionality (microprocessor functions, Arithmetic Logic Unit functions and RAM and ROM memory functions) of the Cypress MicroSystems CY8C25xxx/26xxx series microcontrollers. Detailed information regarding this commercial product is available from Cypress [Micro Systems,] MicroSystems, Inc., in the form of version 1.11 of ["PSoC Designer:] "PSOC DESIGNER: Integrated Development Environment User Guide", which is hereby incorporated by reference in its entirety as background material. While the present invention is described in terms of an ICE system for the above exemplary microcontroller device, the invention is equally applicable to other complex circuitry including microprocessors and other circuitry that is suitable for analysis and debugging using in-circuit emulation. Moreover, the invention is not limited to the exact implementation details of the exemplary embodiment used herein for illustrative purposes.

Please replace the paragraph beginning at page 14, line 19 with the following:

In the present embodiment, the design of microcontroller 232 is implemented using the [Verilog™] VERILOG® language (or other suitable language). Thus, the full functional design description of the microcontroller is available in a software format. In one embodiment base station 218 is based upon the commercially available [Spartan™] SPARTAN® series of FPGAs from Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124. The [Verilog™] VERILOG® description can be used as the input to the FPGA design and synthesis tools available from the FPGA manufacturer to realize the virtual microcontroller 220 (generally after timing adjustments and other debugging). Thus, design and realization of the FPGA implementation of an emulator for the microcontroller (virtual

microcontroller) or other device can be readily achieved by use of the [Verilog™] VERILOG® description along with circuitry to provide interfacing to the base station and the device under test (DUT).

Please replace the paragraph beginning at page 20, line 17 with the following:

Data transfer continues in this manner until the FPGA 220 is fully programmed by virtue of having received the correct amount of data required by the particular FPGA 220 used in base station 218. Thus, each time the host software is initialized, a data transfer to the FPGA 220 occurs to program the FPGA 220 to function in its capacity of a virtual microcontroller (in this embodiment). Once programming ceases, the FPGA 220 operates as a virtual microcontroller (or whatever device is programmed into the FPGA 220 in general). At this point, the interface 214 ceases to function as a unidirectional programming interface and begins to function as a bidirectional communication interface using the programmed operation of the FPGA 220 communicating through its programmed IEEE [1248] 1284 EPP parallel communication interface.

## SUPPORT FOR AMENDMENTS

Support for the amendments herein can be found throughout the specification as originally filed. The present amendment intends to clarify references to trademarks of Cypress MicroSystems, Inc. and others (see, e.g., M.P.E.P. § 608.01(v) and the attached printouts from http://tess.uspto.gov/, notably the "PENTIUM," "VERILOG" and "SPARTAN" trademark registration information therein, and http://www.cypressmicro.com/corporate/CY_Announces_nov_13_2000.html). No new matter is introduced.